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(54) **WAFER-LEVEL FLIPPED DIE STACKS WITH LEADFRAMES OR METAL FOIL INTERCONNECTS**

(71) Applicant: **Invensas Corporation**, San Jose, CA (US)

(72) Inventors: **Ashok S. Prabhu**, San Jose, CA (US); **Rajesh Katkar**, San Jose, CA (US); **Sean Moran**, Burlingame, CA (US)

(73) Assignee: **Invensas Corporation**, San Jose, CA (US)

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H01L 23/552 (2006.01)
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H01L 23/31 (2006.01)

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CPC ***H01L 23/49575*** (2013.01); ***H01L 23/3114*** (2013.01); ***H01L 23/4952*** (2013.01); ***H01L 23/49513*** (2013.01); ***H01L 23/49541*** (2013.01);
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CPC H01L 23/552; H01L 23/49838; H01L 23/49827; H01L 2224/04042; H01L 2224/06156
USPC 257/659
See application file for complete search history.

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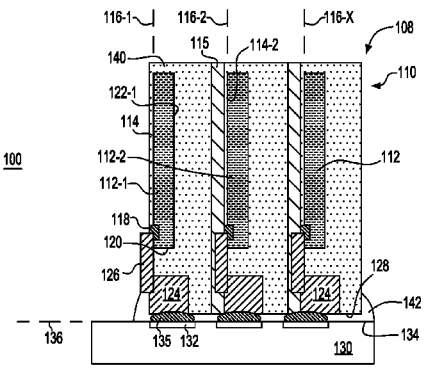
Primary Examiner — Phuc Dang
(74) *Attorney, Agent, or Firm* — Lerner, David, Littenberg, Krumholz & Mentlik, LLP

(57) **ABSTRACT**

An assembly includes a plurality of stacked encapsulated microelectronic packages, each package including a microelectronic element having a front surface with a plurality of chip contacts at the front surface and edge surfaces extending away from the front surface. An encapsulation region of each package contacts at least one edge surface and extends away therefrom to a remote surface of the package. The package contacts of each package are disposed at a single one of the remote surfaces, the package contacts facing and coupled with corresponding contacts at a surface of a substrate nonparallel with the front surfaces of the microelectronic elements therein.

28 Claims, 10 Drawing Sheets



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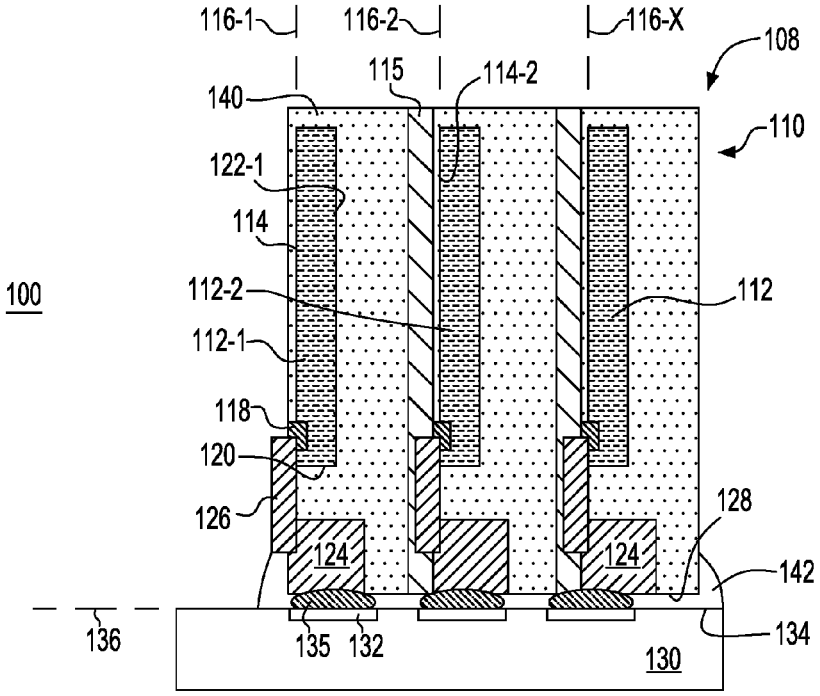

116-1
116-2
116-X
108
115
114-2
140
110
122-1
114
100
112-2
112
112-1
118
120
126
128
124
124
142
136
135
132
134
130

FIG. 1

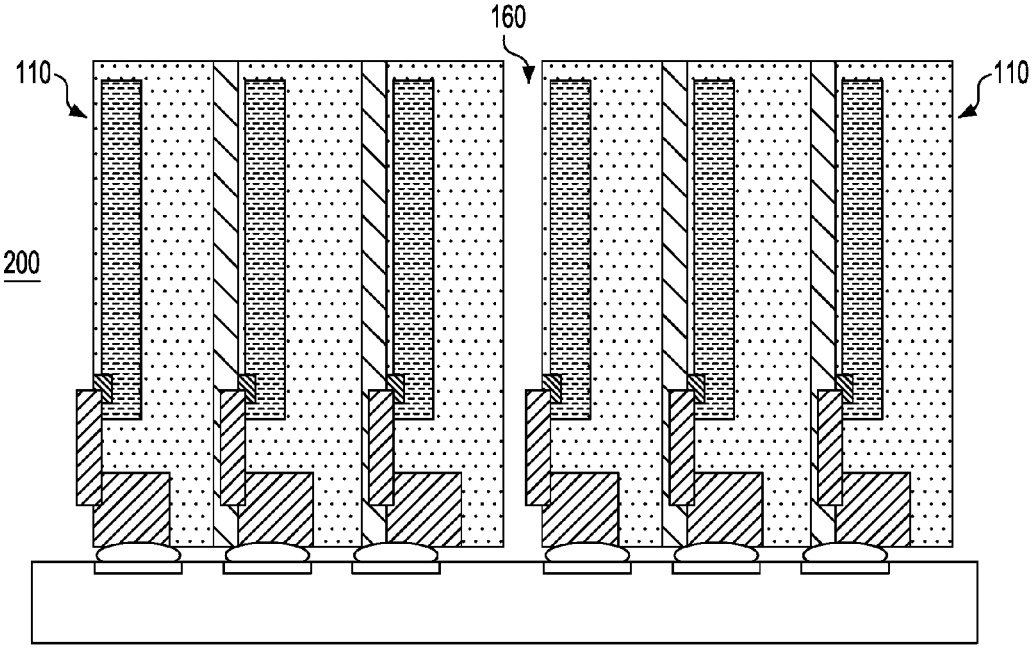

160
110
110
200

FIG. 2

FIG. 3

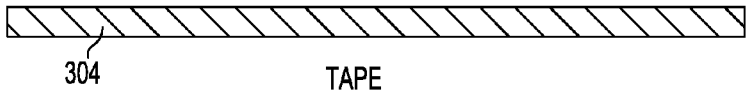


FIG. 4

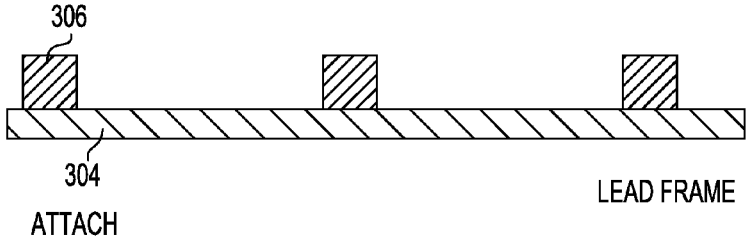


FIG. 5

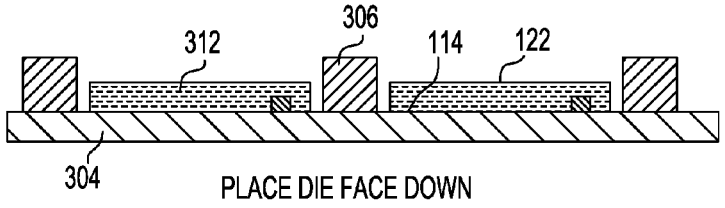


FIG. 6

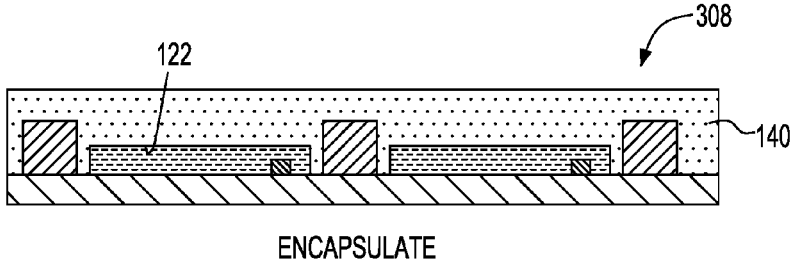


FIG. 7

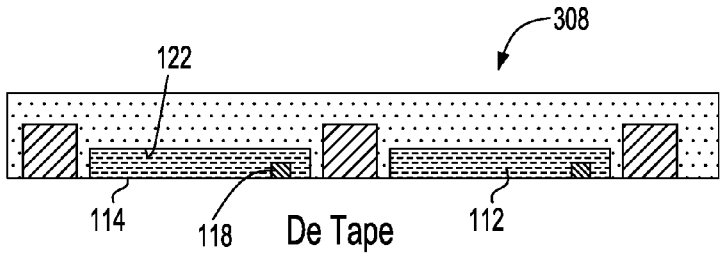


FIG. 8

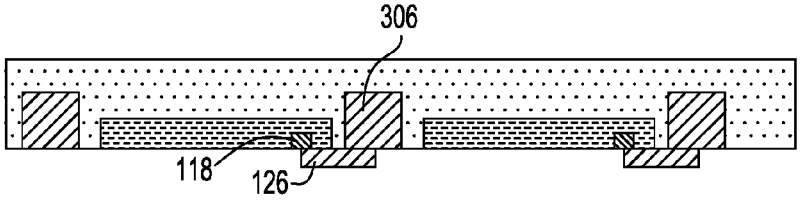


FIG. 9

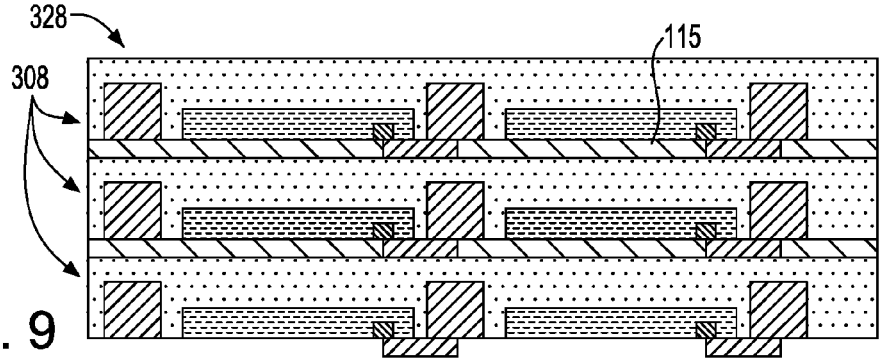


FIG. 10

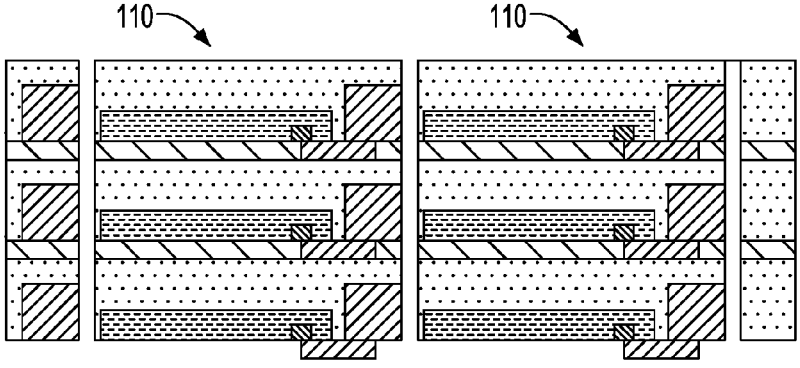


FIG. 11

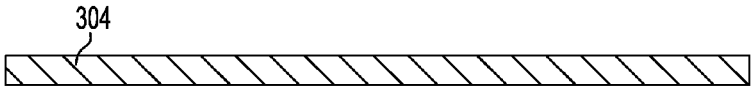


FIG. 12

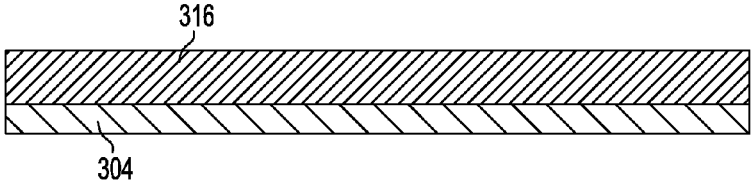


FIG. 13

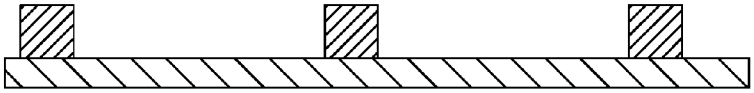


FIG. 14

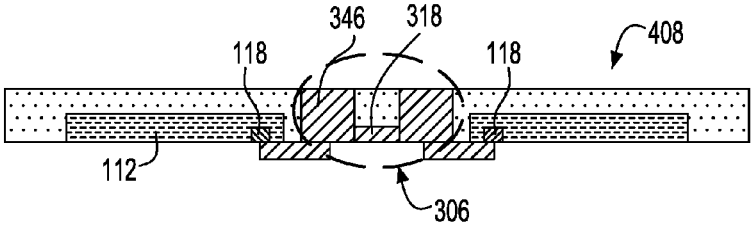


FIG. 15

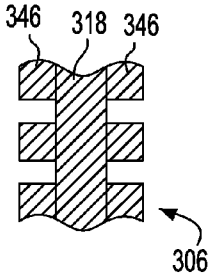
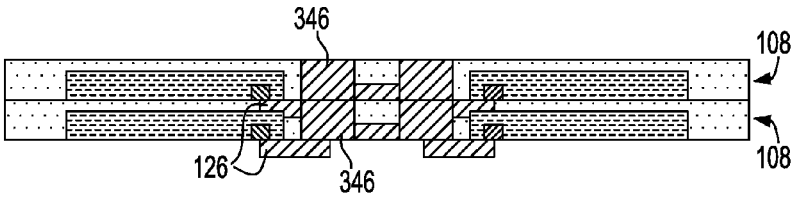


FIG. 16



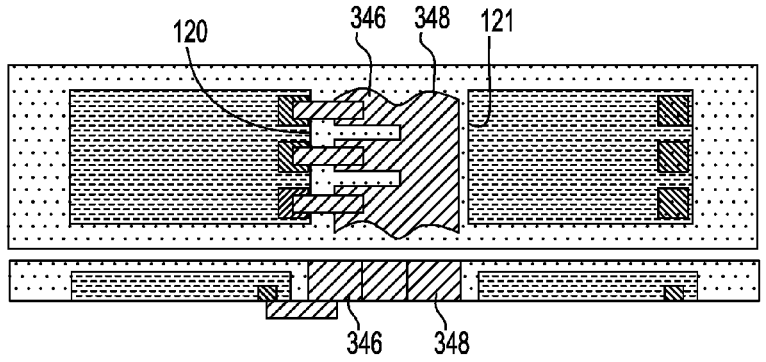


FIG. 17

FIG. 18

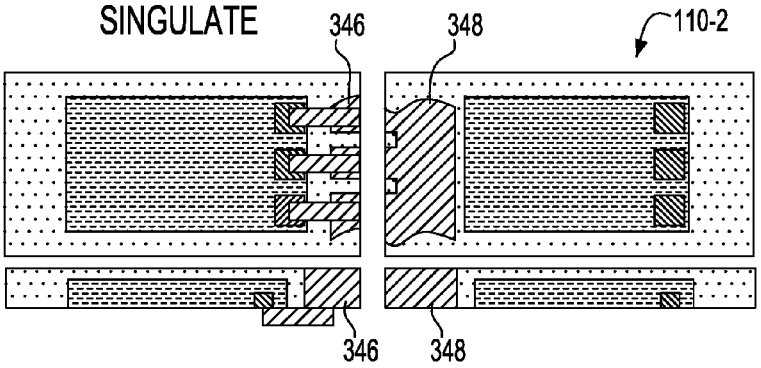


FIG. 19

FIG. 20

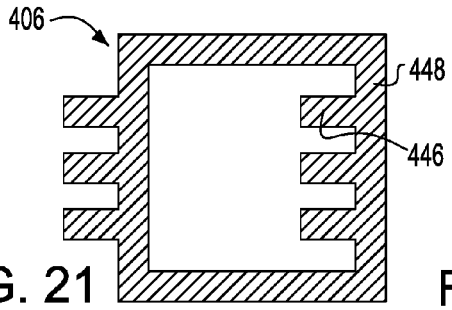


FIG. 21

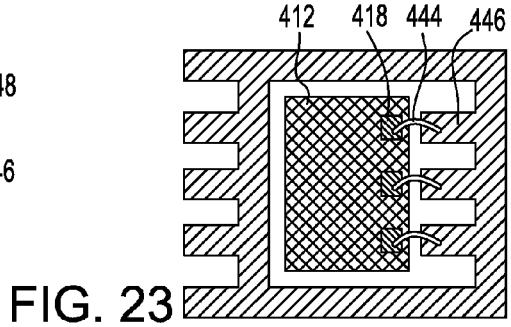


FIG. 23

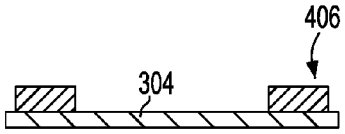


FIG. 22

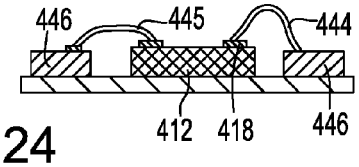


FIG. 24

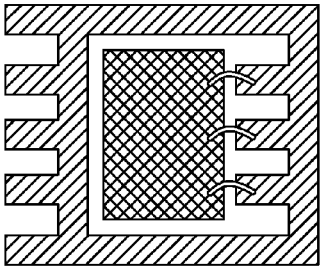


FIG. 25

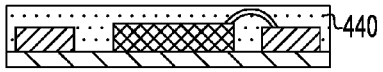


FIG. 26

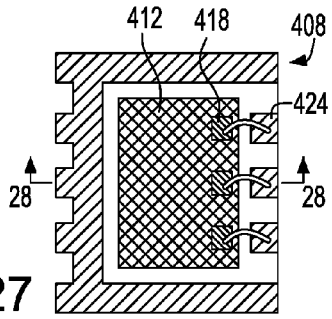


FIG. 27

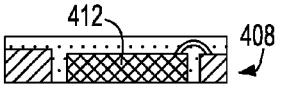


FIG. 28

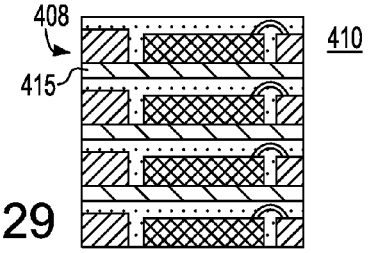


FIG. 29

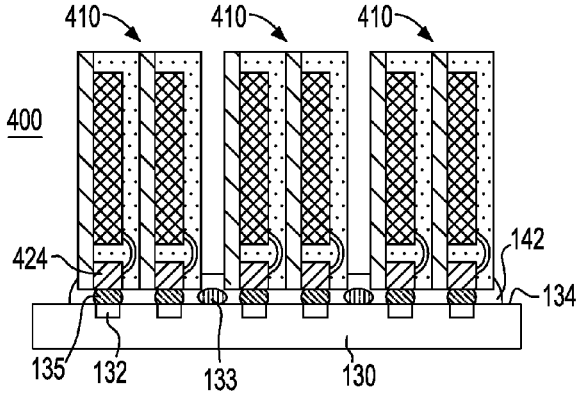


FIG. 30

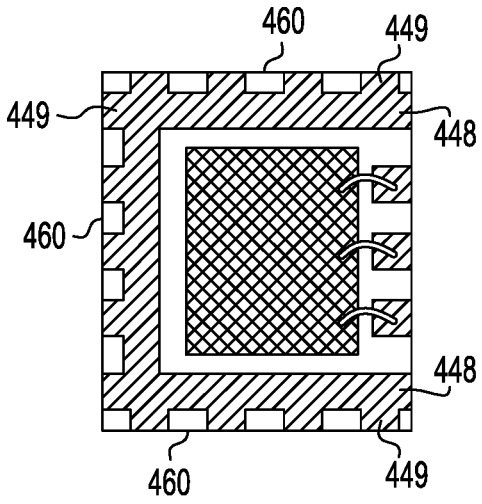


FIG. 30A

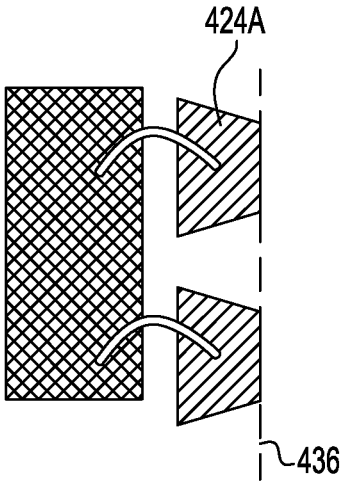


FIG. 30B

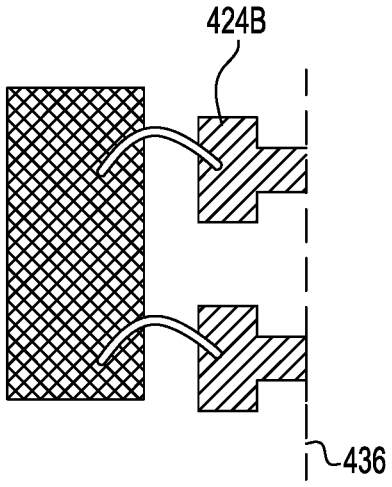


FIG. 30C

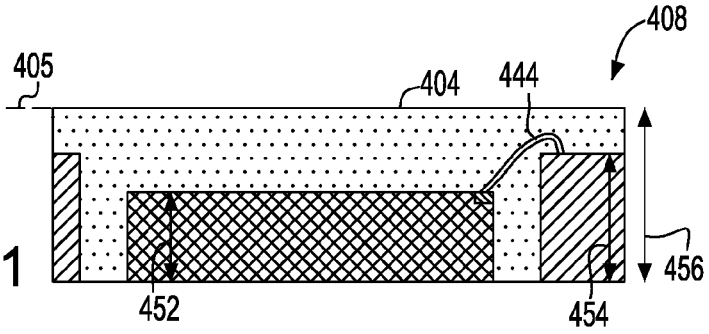


FIG. 31

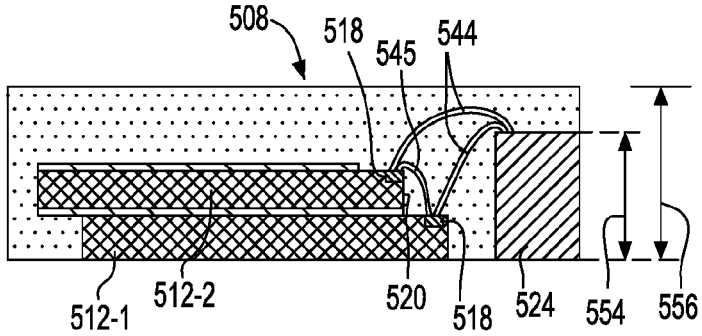


FIG. 32

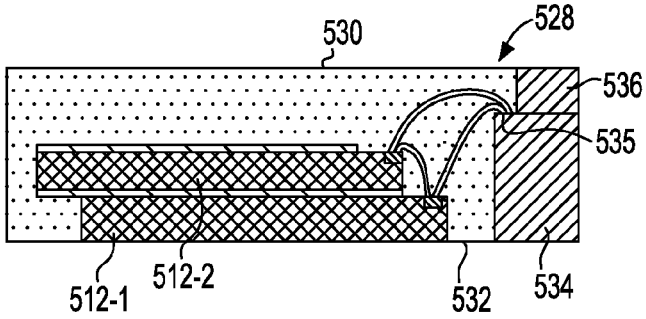


FIG. 34

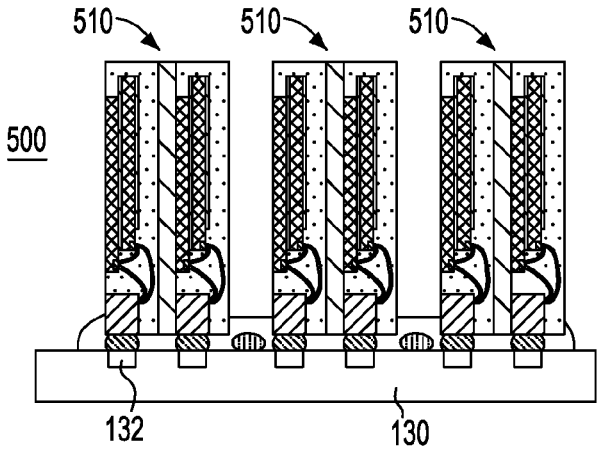


FIG. 33

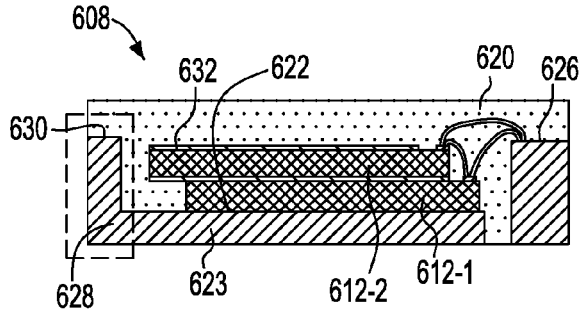


FIG. 35

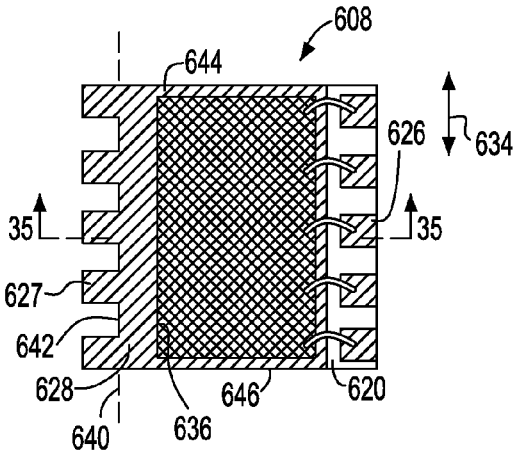


FIG. 36

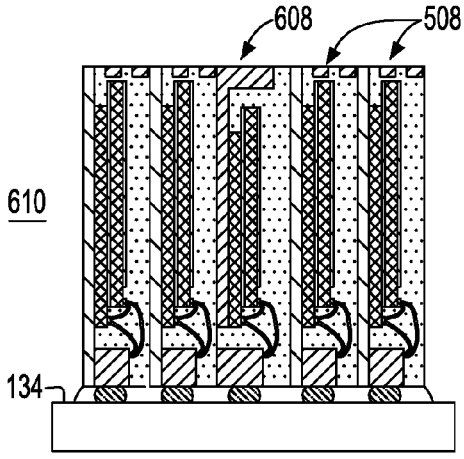


FIG. 37A

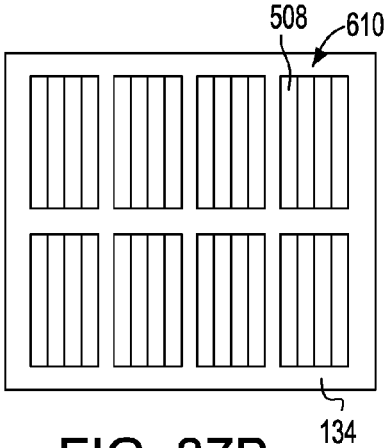


FIG. 37B

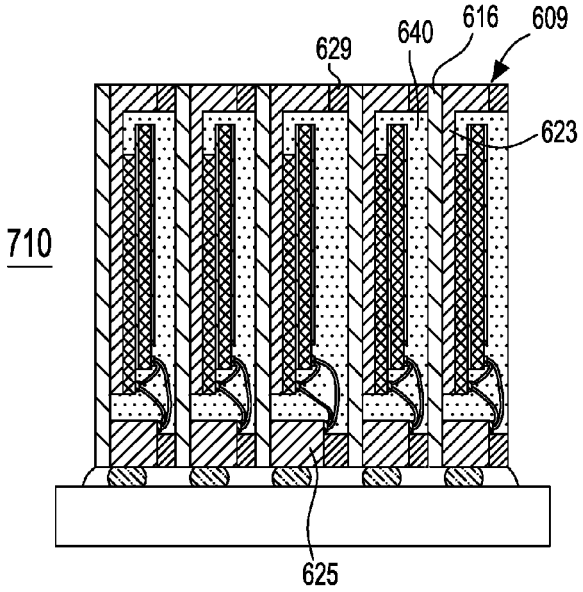


FIG. 38

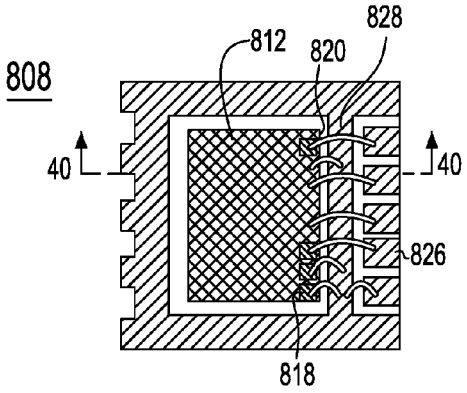


FIG. 39

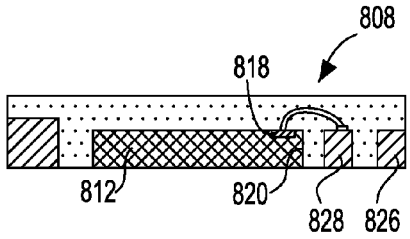


FIG. 40

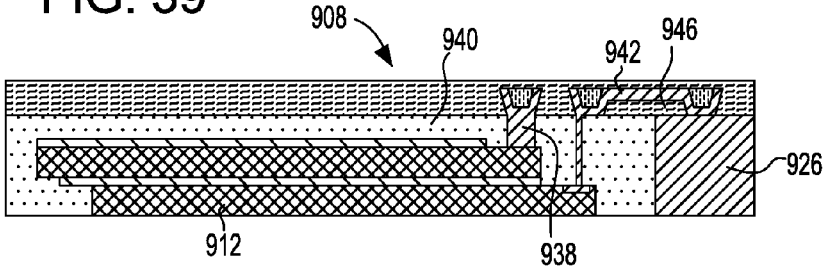


FIG. 41

WAFER-LEVEL FLIPPED DIE STACKS WITH LEADFRAMES OR METAL FOIL INTERCONNECTS

CROSS-REFERENCE TO RELATED APPLICATIONS

This application is a nonprovisional application of U.S. Provisional Application No. 62/222,737 filed Sep. 23, 2015, U.S. Provisional Application No. 62/194,051 filed Jul. 17, 2015 and U.S. Provisional Application No. 62/219,015 filed Sep. 15, 2015, each of the above-indicated nonprovisional applications incorporated by reference herein.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The subject matter of this application relates to microelectronic packages and assemblies in which a plurality of semiconductor chips are stacked one above the other and electrically interconnected with a support element such as a package element or other circuit panel.

2. Description of the Related Art

Semiconductor die or chips are flat bodies with contacts disposed on the front surface that are connected to the internal electrical circuitry of the chip itself. Semiconductor chips are typically packaged with substrates to form microelectronic packages having terminals that are electrically connected to the chip contacts. The package may then be connected to test equipment to determine whether the packaged device conforms to a desired performance standard. Once tested, the package may be connected to a larger circuit, e.g., a circuit in an electronic product such as a computer or a cell phone.

Microelectronic packages can include wafer level packages, which provide a package for a semiconductor component that is fabricated while the chips are still in a wafer form. The wafer is subjected to a number of additional process steps to form the package structure and the wafer is then diced to free the individual die or chips. Wafer level processing may provide a cost savings advantage. Furthermore, fan-out wafer-level packages can be fabricated by encapsulating edges of an array of semiconductor chips within a reconstituted wafer, and then performing additional processing to form fan-out traces and contacts.

In order to save space certain conventional designs have stacked multiple microelectronic elements or semiconductor chips within a package. This allows the package to occupy a surface area on a substrate that is less than the total surface area of the chips in the stack. However, conventional stacked packages have disadvantages of complexity, cost, thickness and testability.

In spite of the above advances, there remains a need for improved stacked packages and especially stacked chip packages which incorporate multiple chips for certain types of memory, e.g., flash memory. There is a need for such packages which are reliable, thin, testable and that are economical to manufacture.

BRIEF SUMMARY OF THE INVENTION

In accordance with an aspect of the invention, a stacked microelectronic assembly can comprise a plurality of stacked encapsulated microelectronic packages. Each encapsulated microelectronic package may comprise a microelectronic element having a front surface which defines a plane, and a plurality of edge surfaces extending away from the plane of the front surface, the microelectronic element having a plurality of chip contacts at the front surface. Each package has a plurality of remote surfaces, and an encapsulation region contacting at least one edge surface of the microelectronic element and extending in the first direction away from the at least one edge surface to a corresponding one of the remote surfaces. Thus, the encapsulation region has a major surface substantially parallel to the plane of each stacked microelectronic element. A plurality of electrically conductive package contacts are disposed at a single one of the remote surfaces of each package, the chip contacts electrically coupled with the package contacts. The plurality of microelectronic packages can be stacked one above another in the stacked assembly such that the planes of the microelectronic elements are parallel to one another, and the major surfaces of the encapsulation regions of respective microelectronic packages in the stacked assembly are oriented towards one another.

In accordance with one or more particular aspects, the plurality of package contacts of each package in the stacked assembly face and are electrically coupled with a corresponding set of substrate contacts at a major surface of a substrate external to the encapsulation regions of each package of the stacked assembly, wherein the major surface of the substrate is non-parallel with the planes of the microelectronic elements in the stacked assembly.

In accordance with one or more particular aspects, the encapsulation region of each package may contact at least two of the edge surfaces of the microelectronic element of the package, such that at least two of the remote surfaces of the package are defined by surfaces of the encapsulation region which are spaced apart from the corresponding adjacent edge surfaces.

In accordance with one or more particular aspects, at least one of the microelectronic packages includes a plurality of the microelectronic elements stacked with the planes of each microelectronic element parallel to one another, wherein the encapsulation region contacts the edge surfaces of each of the stacked microelectronic elements, and the chip contacts of each of the stacked microelectronic elements are electrically coupled with the package contacts.

In accordance with one or more particular aspects, major surfaces the encapsulation regions of at least two adjacent microelectronic packages in the stacked assembly are separated from one another by a gap of at least 100 microns.

In accordance with one or more particular aspects, an adhesive contacts the remote surfaces of each package at which the package contacts are disposed, the major surface of the substrate and surrounds each of the connections between the package contacts and the substrate contacts, wherein features at at least a portion of the major surface of the substrate aligned with the gap define flow paths configured to convey the adhesive across the gap.

In accordance with one or more particular aspects, the assembly may further include a heat spreader having at least a portion disposed between the encapsulation regions of the at least two adjacent microelectronic packages in the stacked assembly.

In accordance with one or more particular aspects, ends of the package contacts coupled to the microelectronic element of each package extend beyond the remote surface of the encapsulation region of such package.

In accordance with one or more particular aspects, the package contacts comprise leadframe interconnects, the leadframe interconnects electrically coupled with the chip contacts through leads.

In accordance with one or more particular aspects, ends of the leadframe interconnects coupled to the microelectronic element in a respective one of the microelectronic packages are flush with or recessed relative to the remote surface of the encapsulation region.

In accordance with an aspect of the invention, a microelectronic package is provided which includes a plurality of stacked microelectronic elements each microelectronic element having a front surface defining a plane extending in a first direction and a second direction transverse to the first direction, a plurality of edge surfaces extending away from the plane of the front surface, each microelectronic element having a plurality of chip contacts at the front surface. The microelectronic elements are stacked with the planes parallel to one another. The package has a plurality of remote surfaces, and an encapsulation region contacting at least one edge surface of the stacked microelectronic elements and extending in the first direction away from the at least one edge surface to a corresponding one of the remote surfaces. Thus, the encapsulation region has a major surface substantially parallel to the plane of each stacked microelectronic element. A plurality of electrically conductive package contacts are disposed at a single one of the remote surfaces of each package, the chip contacts electrically coupled with the package contacts.

In accordance with one or more particular aspects, the encapsulation region may contact at least two of the edge surfaces of each microelectronic element of the package, such that at least two of the remote surfaces of the package are defined by surfaces of the encapsulation region which are spaced apart from the corresponding adjacent edge surfaces of the microelectronic elements.

In accordance with one or more particular aspects, ends of the package contacts coupled to the stacked microelectronic elements extend beyond the remote surface of the encapsulation region of such package.

In accordance with one or more particular aspects, the package contacts comprise leadframe interconnects, the leadframe interconnects electrically coupled with the chip contacts through leads coupled to the leadframe interconnects. In accordance with one or more particular aspects, the leads comprise at least one of wire bonds or traces.

In accordance with one or more particular aspects, ends of the leadframe interconnects are flush with or recessed relative to the remote surface of the encapsulation region.

In accordance with one or more particular aspects, the edge surfaces of the stacked microelectronic elements are staggered relative to one another.

In accordance with one or more particular aspects, at least one of the stacked microelectronic elements is bonded to a die attach pad underlying a surface of the at least one microelectronic element.

In accordance with an aspect of the invention, a microelectronic package includes a microelectronic element having a front surface defining a plane extending in a first direction and a second direction transverse to the first direction, a plurality of edge surfaces extending away from the plane of the front surface, the microelectronic element having a plurality of chip contacts at the front surface. The package has a plurality of remote surfaces, and an encapsulation region contacting at least one edge surface of the stacked microelectronic elements and extending in the first direction away from the at least one edge surface to a corresponding one of the remote surfaces. Thus, the encapsulation region has a major surface substantially parallel to the plane of each stacked microelectronic element. A plurality of electrically conductive package contacts are disposed at a single one of the remote surfaces of each package, the chip contacts electrically coupled with the package contacts. The package contacts may in some cases be leadframe interconnects.

In accordance with one or more particular aspects, the encapsulation region may contact at least two of the edge surfaces of each microelectronic element of the package, such that at least two of the remote surfaces of the package are defined by surfaces of the encapsulation region which are spaced apart from the corresponding adjacent edge surfaces of the microelectronic elements.

In accordance with one or more particular aspects, ends of the package contacts extend beyond the remote surface of the encapsulation region.

In accordance with one or more particular aspects, ends of the package contacts are flush with or recessed relative to the remote surface of the encapsulation region.

In accordance with one or more particular aspects, the leads comprise at least one of wire bonds or traces.

In accordance with one or more particular aspects, a substantially rigid leadframe element is disposed adjacent an edge surface of the microelectronic element, the leadframe element having a length dimension parallel to and at least as long as the adjacent edge surface. The leadframe element may have substantial cross-sectional area transverse to the length direction such that the leadframe element functions as at least one of a component of a heat spreader thermally coupled to the microelectronic element, or a component of an electromagnetic shield relative to the microelectronic element.

In accordance with one or more particular aspects, the leadframe element may extend parallel to each of at least three edge surfaces of the microelectronic element.

In accordance with another aspect of the invention, a microelectronic package comprises a microelectronic element having front and rear surfaces each defining a plane extending in a first direction and a second direction transverse to the first direction, a plurality of edge surfaces between the planes of the front and rear surfaces, the microelectronic element having a plurality of chip contacts at the front surface. A die attach pad of the leadframe underlies and is bonded to one of the front or rear surfaces of the microelectronic element. The package has a plurality of remote surfaces, and an encapsulation region contacting at least one edge surface of the stacked microelectronic elements and extending in the first direction away from the at least one edge surface to a corresponding one of the remote surfaces. Thus, the encapsulation region has a major surface substantially parallel to the plane of each stacked microelectronic element. A plurality of electrically conductive package contacts are disposed at a single one of the remote surfaces of each package, the chip contacts electrically coupled with the package contacts.

In accordance with one or more particular aspects, the encapsulation region may contact at least two of the edge surfaces of each microelectronic element of the package, such that at least two of the remote surfaces of the package are defined by surfaces of the encapsulation region which are spaced apart from the corresponding adjacent edge surfaces of the microelectronic elements.

In accordance with one or more particular aspects, a portion of the die attach pad which is not overlain by the microelectronic element bonded thereto is disposed at a second one of the remote surfaces other than the interconnect surface.

In accordance with one or more particular aspects, the portion of the leadframe can extend above a height of the die attach pad to at least a height of the package contacts.

In accordance with one or more particular aspects, the portion of the leadframe defines a discontinuous metal surface at at least one of the remote surfaces.

In accordance with one or more particular aspects, the portion of the leadframe extends above a height of the die attach pad to at least a height of the package contacts, the portion enclosing at least three adjoining edge surfaces of the microelectronic package.

In accordance with one or more particular aspects, the package contacts comprise features configured to avoid release of the package contacts at the interconnect surface of the encapsulation region.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

FIG. **1** is a sectional view depicting a microelectronic assembly in accordance with an embodiment of the invention.

FIG. **2** is a sectional view depicting a microelectronic assembly in accordance with an embodiment of the invention.

FIGS. **3** through **10** are sectional views each depicting stages in a method of fabricating a microelectronic assembly in accordance with an embodiment of the invention.

FIGS. **11** through **13** are each sectional views depicting stages in a method of fabricating a microelectronic assembly in accordance with a variation of the embodiment of the invention depicted in FIGS. **3** through **10**.

FIG. **14** is a sectional view depicting a stage in a method of fabricating microelectronic assembly in accordance with a variation of the embodiment of the invention depicted in FIGS. **3** through **10**.

FIG. **15** is a partial fragmentary top-down plan view corresponding to FIG. **14**.

FIG. **16** is a sectional view depicting a stage in a method of fabricating a microelectronic assembly in accordance with a variation of the embodiment of the invention depicted in FIGS. **3** through **10**.

FIG. **17** is a top-down plan view depicting a stage in a method of fabricating a microelectronic assembly in accordance with a variation of the embodiment of the invention depicted in FIGS. **3** through **10**.

FIG. **18** is a sectional view corresponding to FIG. **17**.

FIG. **19** is a top-down plan view depicting a stage in a method of fabricating a microelectronic assembly in accordance with a variation of the embodiment of the invention depicted in FIGS. **3** through **10**.

FIG. **20** is a sectional view corresponding to FIG. **19**.

FIG. **21** is a top-down plan view depicting a stage in a method of fabricating a microelectronic assembly in accordance with an embodiment of the invention.

FIG. **22** is a sectional view corresponding to FIG. **21**.

FIG. **23** is a top-down plan view depicting a stage in a method of fabricating a microelectronic assembly in accordance with an embodiment of the invention.

FIG. **24** is a sectional view corresponding to FIG. **23**.

FIG. **25** is a top-down plan view depicting a stage in a method of fabricating a microelectronic assembly in accordance with an embodiment of the invention.

FIG. **26** is a sectional view corresponding to FIG. **25**.

FIG. **27** is a top-down plan view depicting a stage in a method of fabricating a microelectronic assembly in accordance with an embodiment of the invention.

FIG. **28** is a sectional view corresponding to FIG. **27**.

FIG. **29** is a sectional view depicting a stage in a method of fabricating microelectronic assembly in accordance with an embodiment of the invention.

FIG. **30** is a sectional view depicting a stage in a method of fabricating microelectronic assembly in accordance with an embodiment of the invention.

FIG. **30**A is a top-down plan view illustrating a stage in a variation of the method illustrated in accordance with FIGS. **21-30**.

FIGS. **30**B and **30**C are fragmentary top-down plan views further illustrating a variation of the method illustrated in accordance with FIGS. **21-30**.

FIG. **31** is a sectional view depicting a microelectronic package according to an embodiment of the invention.

FIG. **32** is a sectional view depicting a microelectronic package according to a variation of the embodiment of the invention depicted in FIG. **31**.

FIG. **33** is a sectional view depicting a microelectronic assembly according to an embodiment of the invention.

FIG. **34** is a sectional view depicting a microelectronic package according to a variation of the embodiment of the invention depicted in FIG. **32**.

FIG. **35** is a sectional view depicting a microelectronic package according to a variation of the embodiment of the invention depicted in FIG. **32**.

FIG. **36** is a top-down plan view corresponding to FIG. **35**.

FIG. **37**A is a sectional view depicting a microelectronic assembly according to an embodiment of the invention.

FIG. **37**B is a top-down plan view depicting a microelectronic assembly according to an embodiment of the invention.

FIG. **38** is a sectional view depicting a microelectronic assembly according to a variation of the embodiment of the invention depicted in FIG. **37**A.

FIG. **39** is a top-down plan view depicting a microelectronic package in accordance with an embodiment of the invention.

FIG. **40** is a sectional view corresponding to FIG. **39**.

FIG. **41** is a sectional view depicting a microelectronic package in accordance with a variation of an embodiment of the invention depicted in FIG. **32**.

DETAILED DESCRIPTION OF THE INVENTION

As used in this disclosure with reference to a dielectric region or a dielectric structure of a component, e.g., circuit structure, interposer, microelectronic element, capacitor, voltage regulator, circuit panel, substrate, etc., a statement that an electrically conductive element is "at" a surface of the dielectric region or component indicates that, when the surface is not covered or assembled with any other element, the electrically conductive element is available for contact with a theoretical point moving in a direction perpendicular to that surface of the dielectric region from outside the dielectric region or component. Thus, a terminal or other conductive element which is at a surface of a dielectric region may project from such surface; may be flush with such surface; or may be recessed relative to such surface in a hole or depression in the dielectric region.

FIG. **1** illustrates a microelectronic assembly **100** in accordance with an embodiment of the invention. As seen in FIG. **1**, microelectronic assembly **100** includes a package stack **110** which includes a plurality of stacked microelectronic subassemblies or microelectronic packages **108**, each

microelectronic subassembly including one or more microelectronic elements **112** such as a semiconductor chip. Microelectronic assembly **100** and other microelectronic assemblies disclosed or referenced herein can provide enhanced storage density which can be especially advantageously provided in systems used in data centers, among which include enterprise systems, government systems, hosted systems, search engine systems, cloud storage, or other large-scale data centers.

In one example, microelectronic element **112** may be a stack of one or more semiconductor chips. In one example, each of the semiconductor chips may include one or more memory storage arrays, which may include a particular memory type such as nonvolatile memory. Nonvolatile memory can be implemented in a variety of technologies some of which include memory cells that incorporate floating gates, such as, for example, flash memory, and others which include memory cells which operate based on magnetic polarities. Flash memory chips are currently in widespread use as solid state storage as an alternative to magnetic fixed disk drives for computing and mobile devices. Flash memory chips are also commonly used in portable and readily interchangeable memory drives and cards, such as Universal Serial Bus (USB) memory drives, and memory cards such as Secure Digital or SD cards, microSD cards (trademarks or registered trademarks of SD-3C), compact flash or CF card and the like. Flash memory chips typically have NAND or NOR type devices therein; NAND type devices are common. Other examples of semiconductor chips **112** may also include one or more DRAM, NOR, microprocessor, controller die, etc. or combinations thereof. Each semiconductor chip may be implemented in one of various semiconductor materials such as silicon, germanium, gallium arsenide or one or more other Group III-V semiconductor compounds or Group II-VI semiconductor compounds, etc. The microelectronic elements **112** in one or more microelectronic subassemblies **108** and in one or more "package stacks" **110** may be a combination of different chip functionalities as described above and a combination of various semiconductor materials as described above. In one embodiment, a microelectronic element may have a greater number of active devices for providing memory storage array function than for any other function.

Each microelectronic element, e.g., semiconductor chip **112** has a front surface **114** defining a respective plane **116-*x*** of a plurality of planes **116-1**, **116-2**, etc. Each semiconductor chip **112** has a plurality of contacts **118** at its front surface and an edge surface **120** which extends away from the front surface of such chip. Each chip also has a rear surface **122** opposite from its front surface **114**.

Although the front surfaces of each of the chips in the package stack are shown all oriented in the same direction in FIG. **1**, the front surfaces of one or more of the chips in the package stack can be oriented in the opposite direction such that the front surfaces of at least two of the chips which are adjacent one another would either face each other or would face in opposite directions away from one another.

In the example seen in FIG. **1**, each package stack **110** may include a dielectric region **115** that extends between the rear surface **122-1** of a first chip **112-1** and a rear surface or front surface **114-2** of a second chip **112-2** that is adjacent to the first chip in the package stack. Such dielectric regions are disposed between adjacent surfaces of other chips in the package stack depicted in FIG. **1**. The dielectric region may include one or more adhesive layers or other dielectric material. Typically, the dielectric region includes at least adhesive layers coupled to each of the opposed front or rear surfaces of adjacent chips in the package stack. In one embodiment, the dielectric region **115** includes one or more layers of epoxy, elastomer, polyimide or other polymeric material.

The package stack also includes a plurality of package contacts which may be defined by metal leadframe interconnects **124** electrically coupled to a chip contact **118** on a microelectronic element through a lead. As seen in FIG. **1**, each package contact can be electrically coupled with the chip contact **118** at a front surface of a microelectronic element through a trace **126**, the trace extending in a direction generally parallel to the front surface **114** towards an edge surface **120** of the respective chip. The traces can be formed by depositing an electrically conductive material. For example, the traces can be formed by plating a metal onto and in-between the contacts **118** and the leadframe **306** (See FIG. **4** and process description below), wherein the leadframe can serve as an electrical commoning element in a process that includes electrolytic plating. In some embodiments, a seed layer therefor can be formed by electroless plating or sputtering. Alternatively, the traces **126** can be formed by depositing drops, droplets or lines of electrically conductive polymer material or electrically conductive ink, or alternatively by blanket depositing such material and then removing the material between laterally adjacent contacts on the same microelectronic subassembly or package **108**, and between adjacent portions of the leadframe on the same microelectronic package **108**.

As depicted in FIG. **1**, each of the leadframe interconnects **124**, each of which is coupled to a chip contact of at least one microelectronic element of a respective package **108**, may extend to a peripheral edge **128** or "remote surface" of the respective package **108**. A dielectric region or encapsulant region contacts the chip contacts at the front surface of the package, such that the remote surface **128** is spaced apart from the edge surface of the microelectronic element adjacent to the remote surface. In particular cases, the encapsulant region can extend from two or more edge surfaces of the microelectronic element to corresponding remote surfaces of the package spaced apart from the edge surfaces.

All leadframe interconnects of a package are disposed at the same remote surface of the encapsulation such that the leadframe interconnects face a major surface **134** of a substrate **130** or support element and joined to corresponding substrate contacts at the major surface **134**. The substrate **130** may be a dielectric element or other substrate and which may have one or multiple layers of dielectric material and one or multiple electrically conductive layers thereon. The substrate **130** can be formed of various materials, which may or may not include a polymeric component, and may or may not include an inorganic component. Alternatively, the substrate may be wholly or essentially polymeric or may be wholly or essentially inorganic. In various non-limiting examples, the support element can be formed of a composite material such as glass-reinforced epoxy, e.g., FR-4, a semiconductor material, e.g., Si or GaAs, or glass or ceramic material.

The substrate can be one that has contacts on a lower surface facing away from the microelectronic assemblies, the contacts configured for surface mounting to another component which can be a card, tray, motherboard, etc., such as via a land grid array (LGA), ball grid array (BGA), or other technique. In another example, the substrate can be a card component having slide contacts on top and bottom surfaces thereof, such as for insertion into a socket. In yet another example, another component such as universal serial bus (USB) controller or other communications controller

can be mounted to the substrate and electrically coupled with the microelectronic assembly, such component assisting in or controlling a flow of information between the microelectronic assembly and a system.

As seen in FIG. **1**, electrically conductive material **135** such as conductive masses, conductive pillars, stud bumps or other suitable electrically conductive material may be used to electrically connect each of the leadframe interconnects **124** at an end thereof to a corresponding substrate contact **132**. Here, the conductive material **135** can be in form of electrically conductive bumps such as masses of solder, tin, indium or eutectic material, or drops or droplets of electrically conductive polymer material or electrically conductive ink on surfaces of the substrate contacts and contacting the leadframe interconnects **124**.

The electrically conductive material may be applied thereto through a transfer mold of solder bumps, balls or features, or application of solder balls, for example, or may alternatively be deposited on the substrate contacts by plating or depositing a metal or other conductive material. Alternatively, the electrically conductive material **135** can be applied by depositing an electrically conductive ink or paste or an electrically conductive polymer material onto an exposed surface of the substrate contact **132**.

Support element **130** may be organic substrate or semiconducting materials like Si, GaAs, etc. As seen in FIG. **1**, the parallel planes **116**-*x* defined by the front surfaces of the chips **114** are oriented transverse to, i.e., in a direction non-parallel to, a plane **136** defined by the major surface **134** of the support element.

In the example shown in FIG. **1**, a dielectric region **140** which in some cases may be made of or include an encapsulant material, overlies the edge surface **120** of a respective chip. Each chip may have such dielectric region overlying the edge surface thereof. In an example, the dielectric region **140** may be or may include a molded dielectric region. In one example, the dielectric region may comprise a polymeric dielectric material, or alternatively a polymeric dielectric material with a filler therein which may have a lower coefficient of thermal expansion than the polymeric material. In some examples, the filler may include particles, flakes or a mesh or scaffold of an inorganic material such as a glass, quartz, ceramic or semiconductor material, among others.

As illustrated in FIG. **1**, the parallel planes **116**-*x* may be oriented in a direction orthogonal to the plane **136** of the support element major surface. FIG. **1** shows an example in which the major surface **134** of the support element faces the edge surfaces **120** of each chip. An adhesive **142**, which may be an underfill, may be applied surrounding the electrical connections between the leadframe interconnects and the substrate contacts and the adhesive may have a function to mechanically reinforce or stiffen such electrical connections and may help the electrical connections withstand stresses due to differential thermal expansion between the chips **112** and the support element **130**.

Referring to FIG. **2**, in a microelectronic assembly **200** according to variation of the embodiment seen in FIG. **1**, a plurality of the microelectronic stacks **110** can be mounted and electrically connected to the substrate contacts **132**. The distance in an orthogonal direction between respective package stacks **110** defines a gap **160** which, in some cases may be 100 microns, or may range from 100 to 200 microns in dimension, or may have a greater value.

Within gap **160** an adhesive can be provided, and/or other elements, which may in some cases include a heat spreader as further describe below, or passive components, hardware, or other components which may or may not be electrically interconnected with one or more of the package stacks **110**.

In the above embodiments shown in FIG. **1** and FIG. **2**, the leadframe interconnects **124** may extend to and be flush with a peripheral edge surface **128** of the dielectric region **140** of the microelectronic package. Alternatively, in other embodiments which are not specifically shown in FIG. **1** or FIG. **2**, the leadframe interconnects may be recessed relative to the peripheral edge surface **128**, or may extend beyond the peripheral edge surface **128**. In a particular variation of such embodiment in which the package contacts such as leadframe interconnects **124** project beyond the peripheral edge surface **128**, provision can be made for the projecting leadframe interconnects **124** to be inserted into one or more corresponding features of the support element **130**, or embedded in the support element. Referring to FIG. **3** et seq., stages in a method of fabricating a microelectronic assembly will now be described. As seen therein, a leadframe **306** is attached to an adhesive tape **304** such as may be used for dicing or other temporary placement of components during manufacturing and assembly. The tape and leadframe may extend beyond that shown in FIGS. **3-4** to encompass a larger area, such as that of a panel, e.g., which typically has dimensions of 500 millimeters by 500 millimeters.

Next, as shown in FIG. **5**, a plurality of microelectronic elements **312** are attached or otherwise placed face-down towards the tape **304** at locations between portions of the leadframe **306**. The front surfaces **114** of the microelectronic elements face toward the tape **304** and the rear surfaces **122** face away therefrom. Thereafter, a dielectric material **140** is applied into spaces between the microelectronic elements **312** and the leadframe to form a reconstituted panel **308**. Typically, the dielectric material covers the rear surfaces **122** and the lead frame as seen in FIG. **6**, but this need not be so in other embodiments. The dielectric material typically is an encapsulant as described above, and in some examples can be applied by a molding process to form a molded dielectric encapsulation.

As further seen in FIG. **7**, the tape **304** is removed, leaving the reconstituted panel **308** shown therein with the front faces **114** and contacts **118** of the microelectronic elements **112** exposed. Thereafter, as seen in FIG. **8**, the above-described electrically conductive traces **126** are formed which electrically connect the contacts **118** with portions of the leadframe **306** adjacent thereto.

Referring to FIG. **9**, a plurality of the reconstituted panels **308** are stacked one atop the other with an adhesive or other dielectric layer **115** between adjacent panels to form a stacked panel assembly **328**. In a particular embodiment, the dielectric layer **115** can be omitted when other structure such as a fixture or frame mechanism maintains the positions of the reconstituted panels relative to one another. Thereafter, as seen in FIG. **10**, the stacked panel assembly is singulated into individual "package stacks" **110**, each package stack **110** being as described above relative to FIG. **1**. The package stacks **110** then are assembled with respective support elements **130** to form the assemblies **100**, **200** seen in FIG. **1** or FIG. **2**.

In another sequence, the reconstituted panel **308** with electrical conductive traces **126** on them (FIG. **8**) can be singulated first to form individual microelectronic packages. These individual packages are then stacked one atop the other with an adhesive or other dielectric layer **115** between adjacent packages to form a microelectronic stack **110**. The

microelectronic stacks **110** then are assembled with respective support elements **130** to form the assemblies **100**, **200** seen in FIG. **1** or FIG. **2**.

Referring now to FIGS. **11-13**, in a variation of the above-described method, instead of attaching a leadframe to an adhesive tape, a metal sheet **316**, e.g., a foil of copper or a foil having a layered metal structure which includes a foil of copper can be attached to an adhesive tape. Leadframes typically have a thickness of 100 micrometers (hereinafter "microns") in a direction orthogonal to the faces of the microelectronic element. The metal sheet **316**, in some cases, can be made thinner than the leadframe, for example, ranging from 1 to 99 microns in thickness. Alternatively, the metal sheet **316** can be made thicker than a typical leadframe. Also, the metal sheet in some cases can be pre-patterned prior to being attached to the tape **304**. FIG. **13** illustrates the metal sheet after patterning performed subsequent to attaching the metal sheet to the tape **304**. Thereafter, the same processing as described above is performed to fabricate a microelectronic assembly **100** or **200** as seen in FIG. **1** or FIG. **2**. In such case, the words "leadframe interconnect" as used herein refer to portions of such metal sheet **316** which remain in the final microelectronic assembly **100** fabricated in this manner.

FIG. **14** illustrates a microelectronic subassembly **408** formed in a variation of the above-described process. In this case, the contacts **118** on adjacent microelectronic elements **112** are disposed near edges of the microelectronic elements such that contacts **118** on an adjacent pair of microelectronic elements are proximate to one another. Thus, the traces **126** extend from the contacts on each of the adjacent microelectronic elements to the leadframe or metal sheet disposed between the adjacent microelectronic elements. As also seen in FIG. **14** and in the partial fragmentary view of FIG. **15**, the leadframe **306** or metal sheet can be patterned prior to forming the encapsulation such that portions **318** of the leadframe **306** or metal sheet disposed between fingers **346** of the leadframe **306** have smaller thickness than the fingers **346**. As used herein, "fingers" refer to laterally extending portions of the leadframe **306** or of a metal sheet **316** prior to singulation into the package stacks **110** seen in FIG. **10**. Providing the smaller thickness may improve subsequent processing such as the cutting process described above relative to FIG. **10** where the cutting instrument can cut through the portions **318** having the smaller thicknesses.

FIG. **16** illustrates a further variation in which individual microelectronic subassemblies **108** are directly electrically coupled with one another through the leadframe fingers **346** or metal sheet portions, the traces **126**, or both.

FIGS. **17-18** illustrate a further variation in which the leadframe fingers extend laterally from a support element **348** of the leadframe which has substantial width in a direction extending between the adjacent edges **120**, **121** of the microelectronic elements shown in FIGS. **17-18**. Referring to FIGS. **19-20**, after the singulation described above referring to FIG. **10**, a portion of the support element **348**, severed from the leadframe fingers **346**, now remains as part of the microelectronic package stack **110-2**. In one example, the severed support element **348** may function as an electrical commoning layer for providing a ground or power connection. In a particular example, the severed support element **348** may serve as an embedded heat spreader integrated as a part of microelectronic subassembly **108**. When direct electrical or thermal connections are provided between the severed support elements **348** at each level in the microelectronic package stack **110-2**, an effective heat spreader can be provided for transporting and thermal energy from areas near a support element **130** as seen in FIG. **1** to a top of the assembly remote from the support element.

In another embodiment as seen in FIGS. **21** and **23**, fingers **446** of the leadframe **406** extend from a leadframe support element **448** which encompasses an area of the microelectronic element. FIG. **22** depicts the leadframe **406** or metal sheet disposed on a tape **304** as described above. Referring to FIGS. **23-24**, a microelectronic element **412** is placed face-up on the tape **304** and wire bonds **444** are formed which electrically connect contacts **418** of the microelectronic element with the fingers **446**.

FIG. **24** illustrates two examples of wire bonds. In a first example, the ball-bond for the wire bond **444** is formed on the contact **418** of the microelectronic element and a stitch bond is formed on the finger **446**. In a second example, the ball-bond of the wire bond **445** is formed on the finger **446** and the stitch bond is formed on the contact of the microelectronic element. An assembly having a lower height can be obtained by using a reverse-bonding technique in which the ball-bond is formed on the element which has a substantially lower height than the other element to which it is connected through the wire bond. Depending on whether the microelectronic element or the leadframe has the greater height, reverse-bonding technique can help decrease the loop height of the wire bond, effectively reducing a height of the wire-bonded assembly seen in FIGS. **23-24**.

FIGS. **25-26** illustrate the subassembly after forming a dielectric region **440** thereon, which typically is a dielectric encapsulant such as described above, and which is typically formed by a molding process.

FIGS. **27-28** illustrate subsequent singulation of the subassembly into individual microelectronic packages **408**, each package **408** including a microelectronic element **412** having contacts **418** electrically connected to individual leadframe interconnects **424** formed by separating the leadframe fingers **446** from other portions of the leadframe.

FIG. **29** illustrates a stage in which the individual microelectronic packages **408** have been stacked and assembled together one atop the other to form the microelectronic stack **410**. As seen in FIG. **29**, a dielectric material or adhesive **415** can mechanically bind adjacent microelectronic packages **408** to one another. Alternatively, any of the techniques described above relative to FIG. **1** or FIG. **16**, for example, can be used to maintain the positions of the microelectronic packages relative to one another.

FIG. **30** illustrates an assembly which includes one or more microelectronic package stacks **410** for which the leadframe interconnects **424** of each package stack **410** are electrically coupled with corresponding contacts **132** at a major surface **134** of a support element **130**, e.g., through electrically conductive material **135** as described above. In this case, each package stack **410** is shown including only two microelectronic packages **408**, although each package stack **410** can include a greater number of microelectronic packages **408**. In a variation of the embodiment shown in FIG. **30** (not shown), each microelectronic package **408** can be assembled individually with the support element. FIG. **30** further illustrates a dielectric stiffening material **142**, e.g., an underfill, contacting the remote surfaces of each package at which the package contacts are disposed, and the major surface of the substrate, the stiffening material surrounding each of the connections between the package contacts and the substrate contacts. As further shown, features **133** such as dummy bumps, which can have either electrically conductive or insulating properties, can be disposed at at least a portion of the major surface of the substrate aligned with

a gap between package stacks, such features defining flow paths configured to convey the dielectric stiffening material across the gap.

Referring to FIG. **30**A, in a variation of the embodiment described above relative to FIGS. **21-30**, leadframe elements including leadframe support elements **448** define a discontinuous metal surface at at least one of the remote surfaces **460** of the encapsulation region. In such variation, the extent of cutting required of the leadframe support elements **448** is reduced. In this case, the cutting instrument can be positioned so as to cut through leadframe fingers **449** at peripheral edges of each microelectronic package rather than through leadframe support elements **448** which extend continuously in the same direction as the path of the cutting instrument. With the reduced cutting provided in this way, a blade or other element of the cutting instrument may be subject to less wear, and other benefits such as improved process window, or less production of debris may be achieved.

FIGS. **30**B and **30**C illustrate a further variation in which leadframe interconnects **424**A and **424**B, respectively, may include features, e.g., an advantageous geometry, which assist in locking the leadframe interconnects **424**A or **424**B in place within the dielectric region, e.g., molded dielectric encapsulation of each respective package. With such features, when the cutting instrument severs the leadframe fingers at lines **436** in each example to form the leadframe interconnects **424**A or **424**B, the features—characterized by a widening of a lateral dimension of the leadframe fingers in a direction away from lines **436**—assists in avoiding the leadframe interconnects **424**A, **424**B from being released from their attachments with the molded dielectric encapsulation after such singulation process.

FIG. **31** further depicts the microelectronic package **408** and thicknesses of elements therein in a direction orthogonal to a plane **405** in which a major surface **404** of the package **408** lies. For example, the microelectronic element may have a thickness **452** ranging from 10 to 100 microns. The leadframe interconnect **424** may have a thickness **454** typically of 100 microns when the leadframe interconnect is formed by severing leadframe fingers from a standard leadframe. Although thickness **454** of the leadframe interconnect is shown to be 100 microns, the thickness **454** can be smaller or larger than 100 microns. Given these dimensions and the wire bonds **444** providing the electrical interconnections therein, each microelectronic package **408** may have a thickness **456** of 150-200 microns to account for loop height of the wire bonds **444** extending above top surfaces of the leadframe interconnects.

Given the above dimensions of a microelectronic package **408** which includes a single microelectronic element, an alternative microelectronic package **508** is illustrated in FIG. **32** which includes first and second microelectronic elements **512-1** and **512-2**, each having contacts **518** interconnected via wire bonds **544** with the leadframe interconnects **524**. Typically, the microelectronic elements **512-1** and **512-2** are stacked in a staggered manner such that the contacts **518** on the lower positioned microelectronic element **512-1** are disposed beyond an adjacent edge surface **520** of the higher positioned microelectronic element **512-2**. In one example, corresponding contacts **518** on each microelectronic element **512-1** and **512-2** can each be wire bonded directly to the same leadframe interconnect **524** via wire bonds **544**. In another example, corresponding contacts **518** on the microelectronic element **512-1** and **512-2** can be wire bonded with one another via wire bond **545**, and only one of the microelectronic elements **512-1** or **512-2** can be wire bonded directly to the leadframe interconnect **524**. It is not necessary, although it is possible, for the contacts **518** of each microelectronic element to be both directly wire bonded to the corresponding leadframe interconnect **524**, and to be wire-bonded with one another.

FIG. **33** further illustrates a microelectronic assembly **500** which includes one or more "package stacks" **510** each package stack formed by assembling a plurality of multi-chip microelectronic packages **508** each as described relative to FIG. **32**. The multi-chip packages in each package stack **510** are electrically interconnected with contacts **132** at a surface of a support element **130** in a manner such as described above relative to FIG. **30**.

An advantage of providing more than one microelectronic element electrically coupled with the leadframe interconnects in an individual microelectronic package is a potential to increase a density of interconnection of the microelectronic elements in a microelectronic assembly **500** relative to the contacts **132** of the support element **130**. Thus, microelectronic packages **508** incorporating two chips per package are electrically interconnected with the substrate contacts **132** at an effective pitch which is one half the pitch of interconnection between adjacent microelectronic packages **508** in each package stack **510**. In one example, a thickness **554** of each leadframe interconnect in a vertical direction of the microelectronic package may be 100 microns for a standard leadframe thickness and a thickness **556** of the microelectronic package can be 200 microns, for example. Thus, when the pitch among substrate contacts **132** is 200 microns, because there are two microelectronic elements in each package which are electrically coupled with the leadframe interconnects of such package, the effective pitch of interconnection among adjacent microelectronic elements in each of the package stacks **510** seen in FIG. **33** can be 100 microns. When the microelectronic elements are microelectronic elements having memory storage arrays therein, corresponding chip contacts on all of the microelectronic elements in the package can be electrically coupled with a single package contact of the package. The same can apply to most or all of the chip contacts of each microelectronic element, except for chip contacts assigned to receive signals routed uniquely to one of the microelectronic elements, such as a chip select input, for example. The same applies to microelectronic elements which provide non-volatile memory storage array function, such non-volatile memory storage array implemented by a greater number of active devices in the microelectronic element than for any other function of the microelectronic element.

The number of microelectronic elements stacked one above the other in each microelectronic package can range from a small number such as one or two to a much larger number, for example, eight, ten or even greater. In one example, four microelectronic elements can be stacked within a single package and are electrically coupled with the package contacts, e.g., leadframe interconnects of such package. In another example, eight microelectronic elements can be stacked within a single package and are electrically coupled with the leadframe interconnects, in a variation of the package as seen in FIG. **32**.

Referring to FIG. **34**, in a variation of the above-described microelectronic package, a microelectronic package **528** can include leadframe interconnects **534** which are each at a lower surface **532** and at an upper surface **530** of the microelectronic package and, thus, are available for connection with external components at these lower and upper surfaces **532**, **530**. As shown in FIG. **34**, in this variation, each leadframe interconnect may include a ledge **535** to

which wire bonds are joined and electrically coupled to the contacts of the microelectronic elements **512-1** and **512-2**, and may further include a portion **536** projecting above a height of the ledge **535** and at the upper surface **530** of the microelectronic package.

Referring to FIG. **32** and FIG. **34**, in another variation, a greater number of microelectronic elements can be stacked and electrically interconnected to the leadframe interconnects **534** of a given microelectronic package **508** or **528**. For example, each microelectronic package may include three, four, or an even greater number of microelectronic elements arranged in an offset stack as seen in FIG. **32** or **34** and electrically interconnected with the leadframe interconnects which are provided in such microelectronic package. Thus, referring to an arrangement of microelectronic elements **512-1** and **512-2** as seen in FIG. **32**, a microelectronic package **508** modified in accordance with another arrangement to include four microelectronic elements instead of two would yield an effective pitch of 50 microns for interconnection with each microelectronic element therein.

FIGS. **35** and **36** illustrate a microelectronic package **608** according to a variation of the embodiment described above relative to FIG. **32** in which a chip **612-1** in microelectronic subassembly or package **608** has a major surface **622** bonded to a major surface of a metal die attach pad **623** portion of the leadframe. As further seen in FIGS. **35** and **36**, the major surface of the die attach pad can be recessed below a height of the top surfaces **626** of the leadframe interconnects, and thus may accommodate a height of the topmost front surface of one or more microelectronic elements **612-1**, **612-2**. Thus, the recessed major surface of the die attach pad accommodates a thickness of a first microelectronic element **612-1** which may be bonded directly to the die attach pad **623**. When a second microelectronic element **612-2** is present and secured indirectly to the die attach pad **623** through the first microelectronic element **612-1**, the recessed major surface of the die attach pad accommodates thicknesses of the first and the second microelectronic elements **612-1** and **612-2**. In addition, as further seen in FIGS. **35-36**, the leadframe may further include a metal member **628** similar to the metal member **348** described above relative to FIG. **20**, but which is mechanically, electrically and thermally connected with the die attach pad **623**, e.g., as a portion integral with or alternatively metallurgically joined with the die attach pad. As further seen in FIG. **36**, the metal member **628** is elongated in a direction **634** which is parallel to an adjacent edge surface **636** of the at least one microelectronic element **612-1** and **612-2** of the package **608**.

After assembly of the microelectronic elements, leadframe, forming electrical interconnections e.g., using wire bonds, a dielectric region **620**, and separating the metal member from leadframe fingers **627** adjacent thereto along a plane **640** to form the microelectronic package **608**, a surface of the metal member within the plane **640** can define an edge surface of the microelectronic package **608**. In addition, the microelectronic package may likewise include additional second and third metal members **644** and **646** which have length elongated in directions parallel to the respective adjacent edges of the microelectronic element. In addition, the metal members **644**, **646** may have surfaces which define edge surfaces of the microelectronic package, and, like metal member **628**, may extend to a greater height than the die attach pad **623** which accommodates the one or more microelectronic elements **612-1** and **612-2** between the height of an upwardly-facing surface of the die attach pad **623** and the height of a top surface **630** of the metal member. In one example, the metal members **644** and **646** are portions of the die attach pad **623** which extend to opposite edges of the die attach pad **623**. In another example, the height of a top surface **630** of the metal member **628**, **644** and/or **646** may be higher or lower than the front or active surface **632** of the microelectronic element **612-2**.

With such variation, the die attach pad and metal members coupled thereto may provide even greater thermal and electrical conductivity, such as for purposes of transferring heat or providing power or ground connectivity. In addition, a structure which includes the die attach pad and one or more of the above-described metal members **628**, **644** and/or **646** may help avoid coupling of unwanted electromagnetic interference between the one or more microelectronic elements **612-1** and **612-2** and the environment external to the metal members.

In addition, the variations described above relative to FIG. **30**A, **30**B or **30**C can be applied to the embodiments described relative to FIGS. **35-36** here.

FIGS. **37**A-B illustrate a microelectronic assembly **610** in accordance with a particular example in which a microelectronic package of the type described above relative to FIGS. **35-36** is combined with other microelectronic packages **508** of the type described above relative to FIG. **32**. In such assembly, the die attach pad **623** with one or more metal members extending therefrom can function as a heat spreader facilitating conduction of thermal energy away from microelectronic elements therein.

As further seen in the top-down view of FIG. **37**B, and in accordance with any of the embodiments herein, a plurality of the microelectronic assemblies, e.g., assembly **610** or **510** (FIG. **33**), among others, can be coupled to contacts at a surface **134** of a substrate. In the particular example, eight microelectronic assemblies are shown, each which includes four microelectronic packages such as the package **508** or **608**, for example. In one embodiment, each encapsulated microelectronic package of each assembly may include one to eight stacked microelectronic elements. In such case, the assembly of the substrate coupled the plurality of eight microelectronic assemblies shown will include from 32 to 256 microelectronic elements. Referring to FIG. **38**, in a microelectronic assembly **710** according to variation of the assembly **610** in FIG. **37**A, a plurality of microelectronic packages **609** are arranged together in a stacked configuration, wherein each microelectronic package **609** is the same as a microelectronic package **608** except in this case, each substantially rigid metal member or leadframe element **629** and each leadframe interconnect **625** extends a full thickness of the microelectronic package **609** in a vertical direction of the microelectronic package. In such structure, the metal members **629** of the microelectronic packages are joined together through with a thermally and/or electrically conductive adhesive material **616** bonding the die attach pad **623** of each package to the metal members and a surface of the dielectric region **640** of another microelectronic package immediately adjacent and below the die attach pad of the respective microelectronic package.

Referring to FIGS. **39-40**, in a microelectronic package **808** according to a further variation of the single-chip or multiple-chip microelectronic packages described above, the microelectronic element has an edge surface **820** along which contacts **818** of the microelectronic element are disposed, and the leadframe includes a metal member **828** parallel to and elongated in a direction of a length of the interconnect edge surface. As specifically depicted in FIG. **39**, the metal member **828** may surround the one or more microelectronic elements **812** within the package and have a ring-like geometry. The metal member may function as an

element for electrical connection of the contacts **818** with ground or to other steady voltage such as a reference voltage or a power supply voltage. As further seen in FIG. **39**, some contacts **818** may be electrically interconnected directly with the metal member, while others of the contacts are electrically interconnected directly with leadframe interconnects **826** which are disposed beyond the metal member and which may be at a periphery of the microelectronic package **808**. Alternatively, some of the leadframe interconnects **826** can be electrically interconnected directly with the metal member **828** and may not have a direct electrical interconnection with a contact **818** of the microelectronic element **812**. As depicted in FIGS. **39-40**, the electrical interconnections between the contacts, the metal member, and the leadframe interconnects can be through wire bonds. However, other interconnection arrangements are possible, such as further described herein.

Referring to FIG. **41**, in a microelectronic package **908** according to a further variation of any of the single-chip or multiple-chip microelectronic packages described above, the contacts **938** of a microelectronic element **912** are electrically interconnected with the leadframe interconnects **926** of the microelectronic package **908** through electrically conductive structure extending above the front surfaces of the microelectronic elements. For example, the electrical interconnections may include vias **938** extending from the contacts and traces **942** extending in a lateral direction relative to the contacts. In other example, the electrical interconnections may include free standing wire bond connections extending from the contacts to the traces **942**, similar to that referred to as bond via array ("BVA") technology such as disclosed, for example, in FIG. 7 of commonly owned U.S. application Ser. No. 13/462,158, now U.S. Pat. No. 8,619,659, incorporated by reference herein. In a specific example illustrated in FIG. **41**, electrically conductive vias **938** can extend through a dielectric region **940** in a vertical direction above the front surfaces of the microelectronic elements and traces **940** can extend above a surface of the dielectric region **940**. In some cases, the traces **942** may contact or be supported on a dielectric layer **946** added above the dielectric region **940**, which may be of a different material than the dielectric region **940**.

In any of the embodiments described herein, the structures and processing above relating to use of a patterned or unpatterned metal sheet can be utilized instead of a leadframe and references to portions of a leadframe such as leadframe fingers, leadframe interconnects, support members and metal members apply equally to portions of such metal sheet.

Although not specifically shown in the Figures or particularly described in the foregoing, elements in the various Figures and various described embodiments can be combined together in additional variations of the invention.

The invention claimed is:

1. A stacked microelectronic assembly, comprising:

a plurality of stacked encapsulated microelectronic packages, each encapsulated microelectronic package comprising:

a microelectronic element having a front surface defining a plane, a plurality of edge surfaces extending away from the plane of the front surface, the microelectronic element having a plurality of chip contacts at the front surface;

an encapsulation region having a major surface substantially parallel to the plane of the microelectronic element and a plurality of remote surfaces extending away from the major surface, and the encapsulation region extending from at least one edge surface of the microelectronic element to at least one of the remote surfaces which overlies the edge surface; and

a plurality of electrically conductive package contacts at a single one of the remote surfaces spaced apart from the corresponding adjacent edge surface of the microelectronic element of the package, the chip contacts electrically coupled with the package contacts,

the plurality of microelectronic packages stacked one above another in the stacked assembly such that the planes of the microelectronic elements are parallel to one another, and the major surfaces of the encapsulation regions of respective microelectronic packages in the stacked assembly are oriented towards one another,

wherein the package contacts are configured for electrically connecting the microelectronic assembly with a corresponding set of substrate contacts at a major surface of a substrate in a state in which the major surface of the substrate is oriented at a substantial angle to the plane of each microelectronic element and is oriented towards each single remote surface of each of the stacked microelectronic packages.

2. The stacked microelectronic assembly as claimed in claim **1**, wherein the plurality of package contacts of each package in the stacked assembly are electrically coupled with the corresponding set of substrate contacts at the major surface of the substrate.

3. The stacked microelectronic assembly as claimed in claim **2**, wherein a package of the stacked microelectronic packages includes a plurality of the microelectronic elements stacked such that the planes of the stacked microelectronic elements of such package are parallel to one another, wherein the encapsulation region of the package is in contact with the edge surfaces of each of the stacked microelectronic elements of the package, and the chip contacts of each of the stacked microelectronic elements of the package are electrically coupled with the package contacts of the at package.

4. The stacked microelectronic assembly as claimed in claim **1**, wherein the encapsulation region of each package contacts at least two of the edge surfaces of the microelectronic element of the package, such that at least two of the remote surfaces of the package are defined by surfaces of the encapsulation region which are spaced apart from the corresponding adjacent edge surfaces.

5. The stacked microelectronic assembly as claimed in claim **1**, wherein ends of the package contacts coupled to the microelectronic element of each package extend beyond the remote surface of the encapsulation region of such package.

6. The microelectronic assembly as claimed in claim **1**, wherein the package contacts comprise leadframe interconnects, the leadframe interconnects electrically coupled with the chip contacts of the package through leads.

7. The microelectronic assembly as claimed in claim **6**, wherein ends of the leadframe interconnects coupled to the microelectronic element in a respective one of the microelectronic packages are flush with or recessed relative to the remote surface of the encapsulation region of such package.

8. A stacked microelectronic assembly, comprising:

a plurality of stacked encapsulated microelectronic packages, each encapsulated microelectronic package comprising:

a microelectronic element having a front surface defining a plane, a plurality of edge surfaces extending

away from the plane of the front surface, the microelectronic element having a plurality of chip contacts at the front surface;

an encapsulation region having a major surface substantially parallel to the plane of the microelectronic element and a plurality of remote surfaces extending away from the major surface, the encapsulation region extending from at least one edge surface of the microelectronic element to at least one of the remote surfaces which overlies the edge surface; and

a plurality of electrically conductive package contacts at a single one of the remote surfaces spaced apart from the corresponding adjacent edge surface of the microelectronic element of the package, the chip contacts electrically coupled with the package contacts,

the plurality of microelectronic packages stacked one above another in the stacked assembly such that the planes of the microelectronic elements are parallel to one another, and the major surfaces of the encapsulation regions of respective microelectronic packages in the stacked assembly are oriented towards one another,

wherein the major surfaces of the encapsulation regions of at least two adjacent microelectronic packages in the stacked assembly are separated from one another by a gap of at least 100 microns, further comprising a heat spreader having at least a portion disposed between the encapsulation regions of the at least two adjacent microelectronic packages in the stacked assembly.

9. The stacked microelectronic assembly as claimed in claim **8**, further comprising an adhesive contacting the remote surfaces of each package at which the package contacts are disposed, the major surface of the substrate, and the adhesive surrounding each of the connections between the package contacts and the substrate contacts, wherein features at the major surface of the substrate aligned with the gap define flow paths configured to convey the adhesive across the gap.

10. A microelectronic package, comprising:

a plurality of stacked microelectronic elements each microelectronic element having a front surface defining a plane extending in a first direction and a second direction transverse to the first direction, a plurality of edge surfaces extending away from the plane of the front surface, each microelectronic element having a plurality of chip contacts at the front surface, the microelectronic elements stacked with the planes parallel to one another;

an encapsulation region having a major surface substantially parallel to the plane of each stacked microelectronic element and having a plurality of remote surfaces extending away from the major surface, the encapsulation region extending from at least one edge surface of the microelectronic element to at least one of the remote surfaces which overlies the edge surface; and

a plurality of electrically conductive package contacts disposed at a single one of the remote surfaces, the chip contacts of each of the stacked microelectronic elements electrically coupled with the package contacts,

wherein the package contacts are configured for electrically connecting the microelectronic package with a corresponding set of substrate contacts at a major surface of a substrate in a state in which the major surface of the substrate is oriented at a substantial angle to the plane of the microelectronic element and is oriented towards the single one of the remote surfaces of the microelectronic package.

11. The microelectronic package as claimed in claim **10**, wherein the package contacts comprise leadframe interconnects, the leadframe interconnects electrically coupled with the chip contacts through leads coupled to the leadframe interconnects.

12. The microelectronic package as claimed in claim **11**, wherein the leads comprise at least one of wire bonds or traces.

13. The microelectronic package as claimed in claim **10**, wherein ends of the package contacts coupled to the microelectronic element of each package extend beyond the remote surface of the encapsulation region of such package.

14. The microelectronic package as claimed in claim **10** wherein ends of the leadframe interconnects are flush with or recessed relative to the remote surface of the encapsulation region.

15. The microelectronic package as claimed in claim **10**, wherein the edge surfaces of the stacked microelectronic elements are staggered relative to one another.

16. The microelectronic package as claimed in claim **15**, wherein at least one of the stacked microelectronic elements is bonded to a die attach pad underlying a surface of the at least one microelectronic element.

17. A microelectronic package, comprising:

a microelectronic element having a front surface defining a plane, a plurality of edge surfaces extending away from the plane of the front surface, the microelectronic element having a plurality of chip contacts at the front surface;

the package having a plurality of remote surfaces, and an encapsulation region contacting at least one edge surface of the microelectronic element and extending away from the at least one edge surface to a corresponding one of the remote surfaces, the encapsulation region having a major surface substantially parallel to the plane of the microelectronic element; and

a plurality of package contacts at a single one of the remote surfaces, the package contacts defined by leadframe interconnects; and

leads electrically coupling the chip contacts of the microelectronic element with the leadframe interconnects, wherein the package contacts are configured for electrically connecting the microelectronic package with a corresponding set of substrate contacts at a major surface of a substrate in a state in which the major surface of the substrate is oriented at a substantial angle to the plane of the microelectronic element and is oriented towards the single remote surface of the microelectronic package.

18. The microelectronic package as claimed in claim **17**, wherein the encapsulation region contacts at least two of the edge surfaces of the microelectronic element of the package, such that at least two of the remote surfaces of the package are defined by surfaces of the encapsulation region which are spaced apart from the corresponding adjacent edge surfaces.

19. The microelectronic package as claimed in claim **17**, wherein ends of the package contacts extend beyond the remote surface of the encapsulation region.

20. The microelectronic package as claimed in claim **17** wherein ends of the package contacts are flush with or recessed relative to the remote surface of the encapsulation region.

21. The microelectronic package as claimed in claim **17**, wherein the leads comprise at least one of wire bonds or traces.

22. The microelectronic package as claimed in claim 17, further comprising a substantially rigid leadframe element adjacent an edge surface of the microelectronic element, the leadframe element having a length dimension parallel to and at least as long as the adjacent edge surface, the leadframe element having substantial cross-sectional area transverse to the length direction such that the leadframe element functions as at least one of a component of a heat spreader thermally coupled to the microelectronic element, or a component of an electromagnetic shield relative to the microelectronic element.

23. The microelectronic package as claimed in claim 22, wherein the leadframe element extends parallel to each of at least three edge surfaces of the microelectronic element.

24. A microelectronic package, comprising:

a microelectronic element having front and rear surfaces each defining a plane, a plurality of edge surfaces between the planes of the front and rear surfaces, the microelectronic element having a plurality of chip contacts at the front surface;

a die attach pad underlying and bonded to one of the front or rear surfaces of the microelectronic element;

the package having a plurality of remote surfaces, and an encapsulation region contacting at least one edge surface of the microelectronic element and extending away from the at least one edge surface to a corresponding one of the remote surfaces, the encapsulation region having a major surface substantially parallel to the plane of the microelectronic element; and

a plurality of package contacts at an interconnect surface being a single one of the remote surfaces, the package contacts electrically coupled with the chip contacts of the microelectronic element, the package contacts defined by leadframe interconnects, wherein a portion of the die attach pad which is not overlain by the microelectronic element bonded thereto is disposed at a second one of the remote surfaces other than the interconnect surface.

25. The microelectronic package as claimed in claim 24, wherein

the portion of the leadframe extends above a height of the die attach pad to at least a height of the package contacts.

26. The microelectronic package as claimed in claim 25, wherein the portion of the leadframe defines a discontinuous metal surface at at least one of the remote surfaces.

27. The microelectronic package as claimed in claim 24, wherein the portion of the leadframe extends above a height of the die attach pad to at least a height of the package contacts, the portion enclosing at least three adjoining edge surfaces of the microelectronic package.

28. The microelectronic package as claimed in claim 24, wherein the package contacts comprise features configured to avoid release of the package contacts at the interconnect surface of the encapsulation region.

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